Docket No. A1WI2376US PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Douglas W. Babcock, Robert A. Duris, Bruce Hecht

Serial No. 10/722,970

Filed: November 25, 2003

Title: AUTOMATIC TEST EQUIPMENT PIN CHANNEL WITH T- COIL COMPENSATION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF ROBERT A. DURIS

I, Robert A. Duris, declare:

1. I am a co-inventor of the invention which is the subject of the above-identified patent application.

2. I was a Senior Staff Engineer for Analog Devices, Inc. (ADI) at all times mentioned herein until my retirement on December 13, 2006.

3. I confirm the Declaration which I signed on May 30, 2006 in connection with the above patent application.

4. On November 30, 1999 I conducted a SPICE (Simulation Program with Integrated Circuit Emphasis) simulation of a circuit that implemented independent claims 1, 7, 22 and 28 of the above patent application with a single T-coil circuit. A schematic diagram of the simulated circuit, which I prepared on November 30, 1999, is attached as Exhibit 1. Attached as Exhibit 2 is a copy

of Exhibit 1 that has been annotated to identify the following elements from claims 1, 7, 22 and 28:

A. Input/output line for connection to a device under test (DUT).

B1. Class-AB (voltage mode) driver circuit connected to apply test signals to said input/output line for application to a DUT.

B2. Class-A (current mode) driver circuit connected to apply test signals to said input/output line for application to a DUT.

C. Receiver circuit connected to said input/output line to receive signals produced by a DUT, said receiver circuit having an associated capacitance (represented by combined parasitic capacitance of the receiver circuit and the Class-A driver circuit).

D. A first passive matching network connected to said line to at least partially compensate for said receiver circuit capacitance, comprising (D1) the inductances of the T-coil circuit coils, (D2) the resistances of the metal coils, (D3) the parasitic capacitances of the two coupled coils, divided into two parts for each coil with one-half placed at each end of each coil, and (D4) a bridge capacitor connected across the two coils of the T-coil circuit.

Elements E and F respectively represent the net bond wire inductance and bond pad capacitance of the input/output line A, while element G represents the DUT.

The simulated circuit of Exhibits 1 and 2 thus embodies all of the elements of independent claims 1, 7, 22 and 28 (the passive matching network D is bidirectional, as required by claims 11 and 17).

5. Exhibits 3A and 3B are plots from the simulation tests which I performed on November 30, 1999 for five different levels of receiver circuit parasitic capacitance, plotted on the same time scale. Fig. 3A is a plot of the DUT voltage, with the region between time = 4.8ns and time = 5.6ns representing the reflected energy of the incident wave from the DUT. Exhibit 3B plots the resulting voltage at the receiver. These plots are tabulated for the five levels of parasitic capacitance in Exhibit 4, in which the terms Tr and Tf refer respectively to rise time and fall time, and Class-A or Class-AB refers to the type of simulated driver circuit used to apply the voltage pulse to the DUT. These results demonstrate that the simulated circuit with a single T-coil successfully compensated for increasing levels of parasitic capacitance in the receiver circuit, and was capable of providing compensation which limited the DUT reflection "bump" to +13.5mV/-38.5mV for a 1pF load.

6. The simulated circuit of Exhibit 1 was later implemented in post-passivation T-coil wafers that were received by ADI on October 12, 2000 and which had two T-coils each, rather than the single T-coil of Exhibit 1. As stated in paragraph 9 of my May 30, 2006 Declaration, ADI developed a characterization setup in its characterization laboratory to test and characterize the drive channel

circuits to which Advanced MicroSystems, an independent company, had added post-passivation T-coils. A circuit with the two post-passivation T-coils was tested on October 17, 2000, and a copy of a trace of the results is attached as Exhibit 5, plotting mp as a function of time. p is a measure of impedance matching; the results show a negative peak of about -120 mp. A similar circuit but without post-passivation T-coils was tested on October 18, 2000, and a copy of a trace of the results is attached as Exhibit 6. This trace shows a negative peak of about -260 mp, which indicated that the addition of the post-passivation T-coils was successful in substantially compensating the receiver circuit capacitance. Both tests were made by Robert Bombara, an ADI employee. These results were consistent with the simulated results of Exhibits 3A, 3B and 4 in demonstrating the success of T-coils in substantially compensating for the receiver circuit capacitance.

7. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 2/26/2007

Robert A. Duris

(U:MR/RSK/Fil/Dec./ R. Duris A1WI2376US)

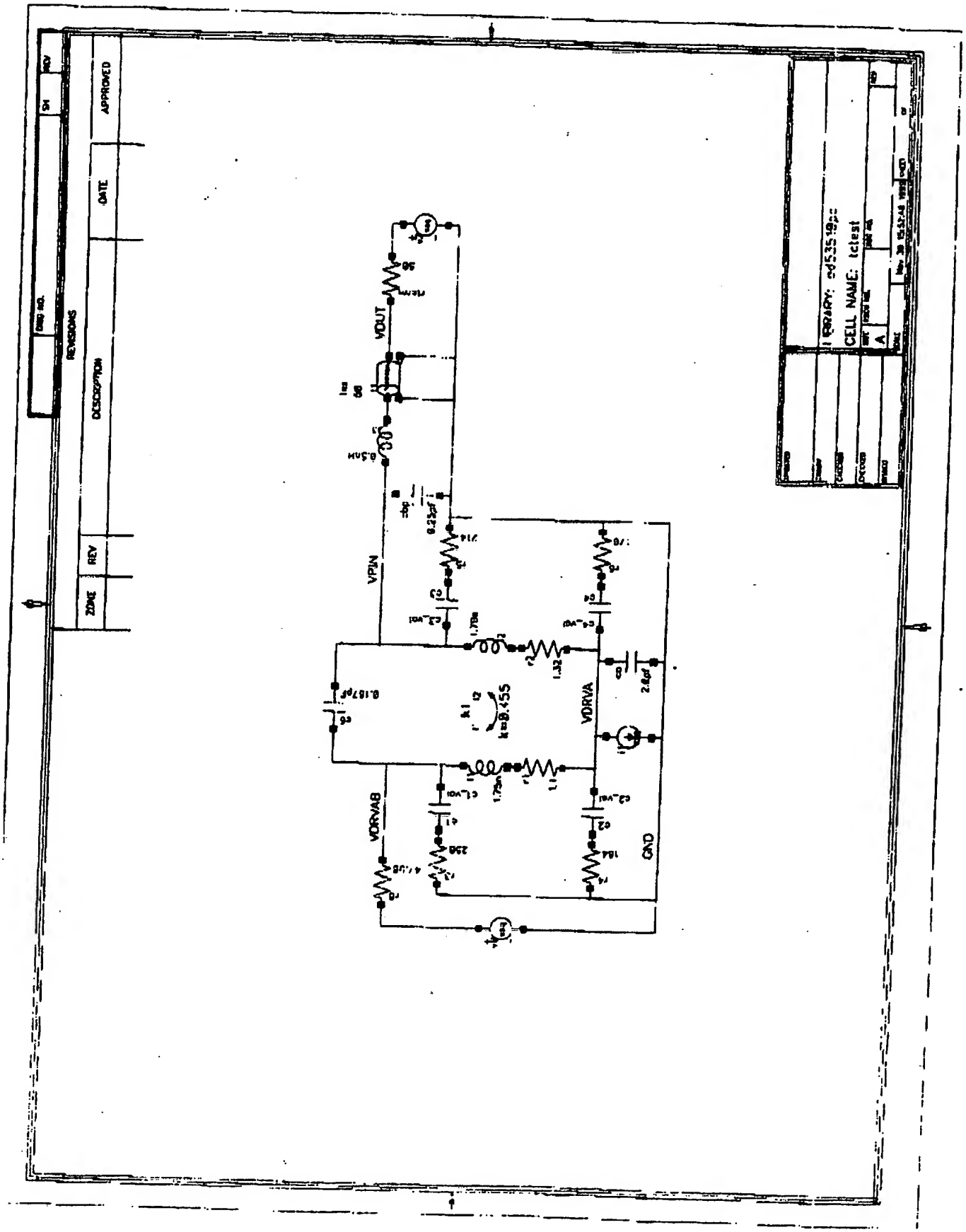


EXHIBIT 1 - DURIS

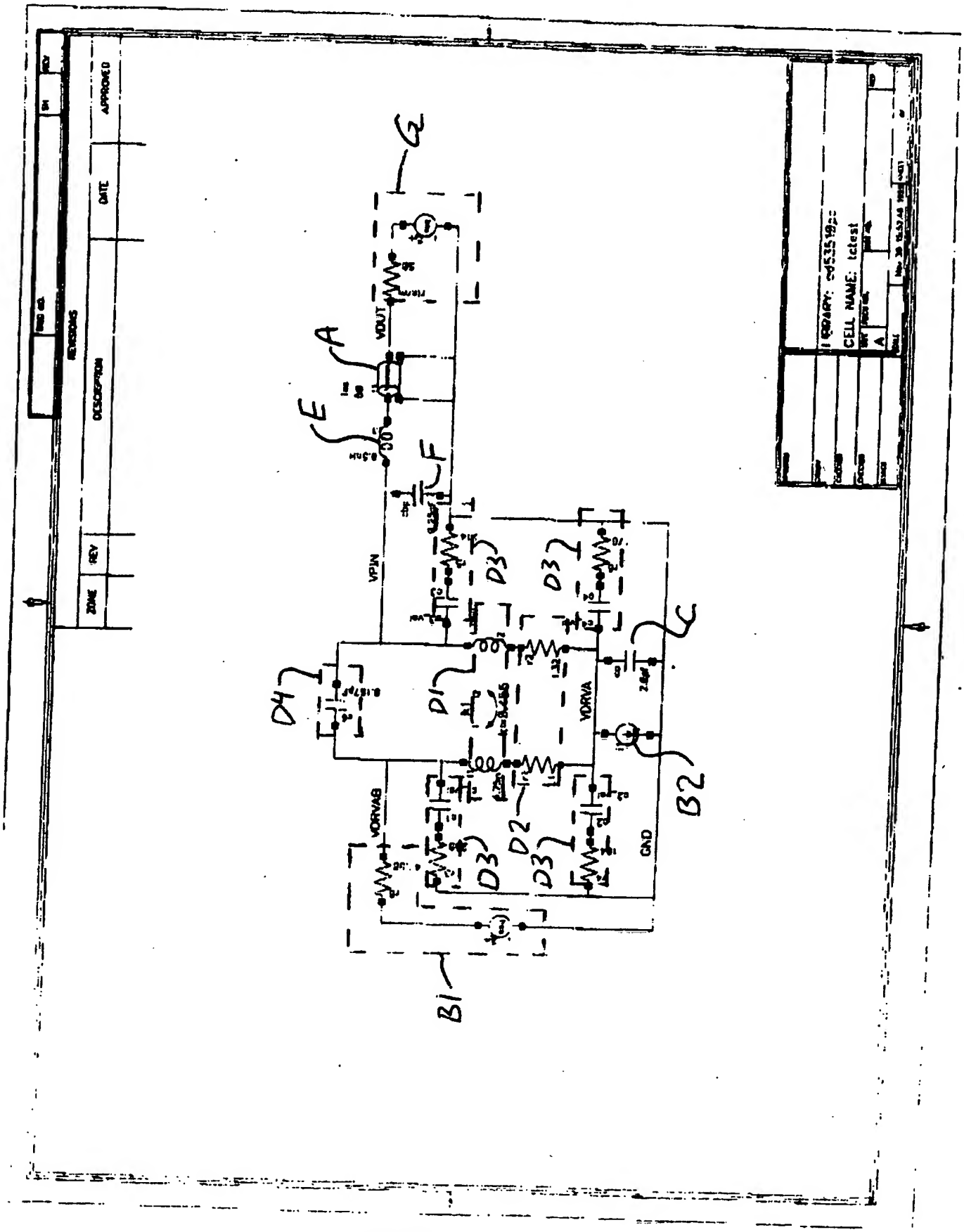
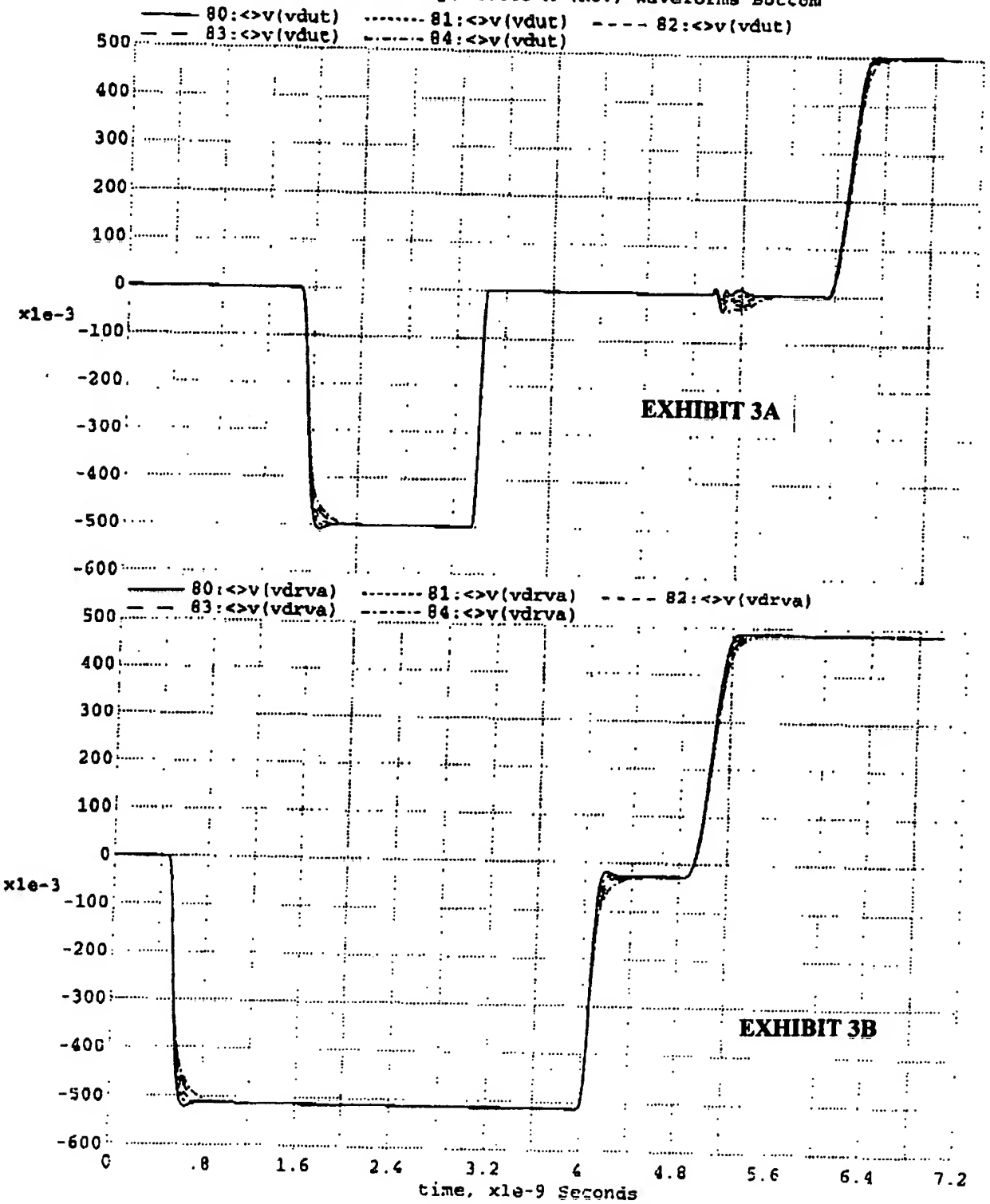


EXHIBIT 2 - DURIS

USER: bduris

30-Nov-99 18:41:37



EXHIBITS 3A, 3B - DURIS

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MET3 T-Coil Simulation Tests

Class A and DUT Input Tr/Tf = 50ps (10/90 SSQ), 0.5V Step (Terminated)
Class AB Input Tr/Tf = 200ps (10/90 SSQ), 0.5V Step (Terminated)

Parasitic Cap Factor	DUT Class-A Tr/Tf	DUT Class-A Overshoot	DUT Reflection Bump	DUT Class-AB Tr/Tf	DUT Class-AB Preshoot	DUT Class-AB Overshoot
0	88ps	8.4mV	13.9 / -9.4mV	200ps	2.3 / -1.2mV	1.5mV
0.25	97ps	0.9mV	13.6 / -21mV	202ps	2.2 / -1.5mV	1.5mV
0.5	106ps	0	13.5 / -29.2mV	206ps	2.1 / -1.7mV	0.1mV
0.75	118ps	0	13.5 / 34.8mV	212ps	2.0 / -1.8mV	0.06mV
1	134ps	0	13.5 / -38.5mV	219ps	2.0 / -1.8mV	0

Parasitic Cap Factor	RCV Class-A Tr/Tf	RCV Class-A Overshoot	RCV Reflection Bump	RCV Class-AB Tr/Tf	RCV Class-AB Preshoot	RCV Class-AB Overshoot	RCV DUT Tr/Tf	RCV DUT Overshoot
0	81ps	8.9mV	---	212ps	0	1.3mV	89ps	7.7mV
0.25	92ps	0.7mV	---	218ps	0	0.2mV	96ps	0.7mV
0.5	105ps	0	---	226ps	0	0	107ps	0
0.75	122ps	0	---	235ps	0	0	118ps	0
1	144ps	0	---	248ps	0	0	136ps	0

Note: Includes 0.25pF bondpad and 0.5nH output bondwire inductance

EXHIBIT 4 - DURIS

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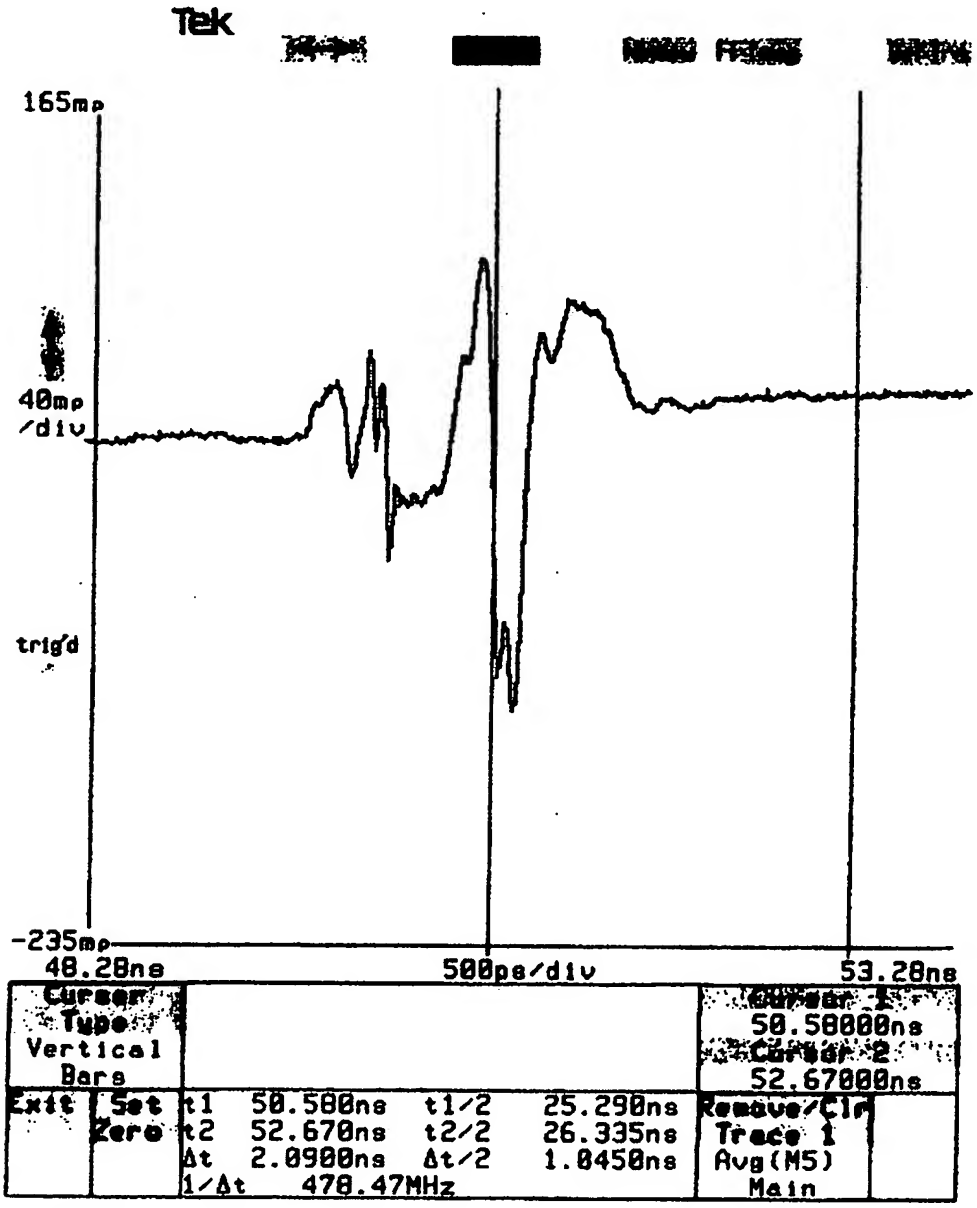

PIN 1

PROBES DOWN

POWER ON

OUT WITH TCOILS

EXHIBIT 5 - DURIS

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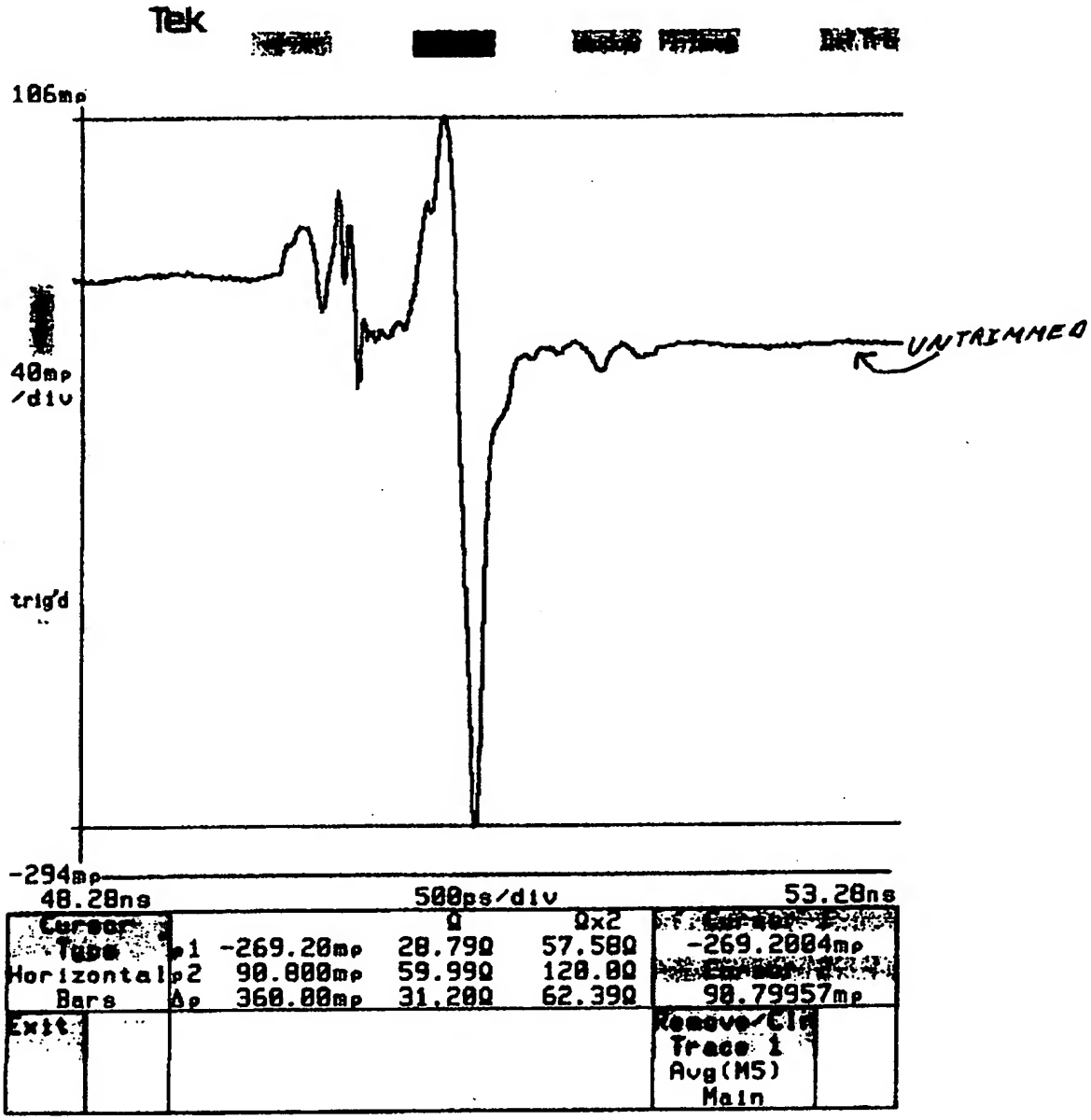

PIN 1
PROBES DOWN
POWER ON
OUT WITHOUT T COILS

EXHIBIT 6 - DURIS